ALPHA DATA

ADM-XRC-6T1
User Manual

Revision: 0.1
Date: 31st May 2010

Contact www.techway.fr

TECHWAY S.A.S.

19 Avenue de Norvège - Bât. Oslo - Villebon-sur-Yvette

91953 Courtaboeuf Cedex - France

T:+33 (0)1 64 53 37 90 - F:+33 (0)1 64 53 17 74

	Head Office	US Office
Address	4 West Silvermills Lane, Edinburgh, EH3 5BD, UK	2570 North First Street, Suite 440 San Jose, CA 95131
Telephone	+44 131 558 2600	(408) 467 5076 General (408) 916 5713 Sales
Fax	+44 131 558 2700	(408) 436 5524 (866) 820 9956 toll free
email	sales@alpha-data.com	sales@alpha-data.com
website	http://www.alpha-data.com	http://www.alpha-data.com

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1 Introduction

The **ADM-XRC-6T1** is a high-performance XMC for applications using Virtex-6 FPGAs from Xilinx™. This card supports all Virtex-6 LXT and SXT devices available in the FF (G)1759 package.

The card includes separate FPGA with a PCIe bridge developed by Alpha Data. Using a separate device allows high performance operation without the need to integrate proprietary cores in the user (target) FPGA.

The **ADM-XRC-6T1** is available in air-cooled and conduction-cooled configurations. View the ADM-XRC-6T1 specification at **ADM-XRC-6T1 Product Page** on **www.alpha-data.com**.

1.1 Key Features

Basic Features

- Single-width XMC, compliant to VITA Standard 42.0 and 42.3,
- Dedicated 4-lane Gen2 PCI-Express interface with 4 high-performance DMA controllers,
- Virtex-6 FPGA in FF(G)1759 package,
- 4 independent banks of DDR3-800 SDRAM, 256MB/bank, 1GB total (2GB option),
- Front-panel (XRM) interface with adjustable voltage, 146 free I/O signals and 8 MGT links to user FPGA,
- Rear-panel (XMC) interface with 38 GPIO signals and 8 MGT links between user FPGA and P6,
- 2 MGT links between user FPGA and P5,
- 2 additional MGT links switchable between user FPGA and P5 or P6,
- Rear-panel (PMC) interface with 64 GPIO signals between user FPGA and P4 (optional)
- Voltage and temperature monitoring (**Section 3.7 'Health_Monitoring'**)

1.2 References & Specifications

ANSI/VITA 42.0	*XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.3	*XMC PCI Express® Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	*IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001 (R2005)	*Conduction Cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4

Table 1: References

2 Installation

2.1 Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2.2 Motherboard / Carrier Requirements

The **ADM-XRC-6T1** is a single width XMC.3 mezzanine with optional P6 and P4 connectors. The motherboard/ carrier must comply with the XMC.3 (VITA 42.3) specification for the Primary XMC connector, J5.

The Secondary XMC connector, J6 has a pinout compatible with VITA 46.9 "X38s + X8d + X12d" mapping.

IMPORTANT: Connector P6 on the card is not compatible with the XMC.10 (GPIO) Standard. In particular, USB VCC must not be applied on this connector.

The **ADM-XRC-6T1** is compatible with either 5V or 12V on the "VPWR" power rail.

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx™ power estimation tools to determine the exact current requirements for each power rail.

2.2.3 Cooling Requirements

t.b.d.

3 Functional Description

3.1 Overview

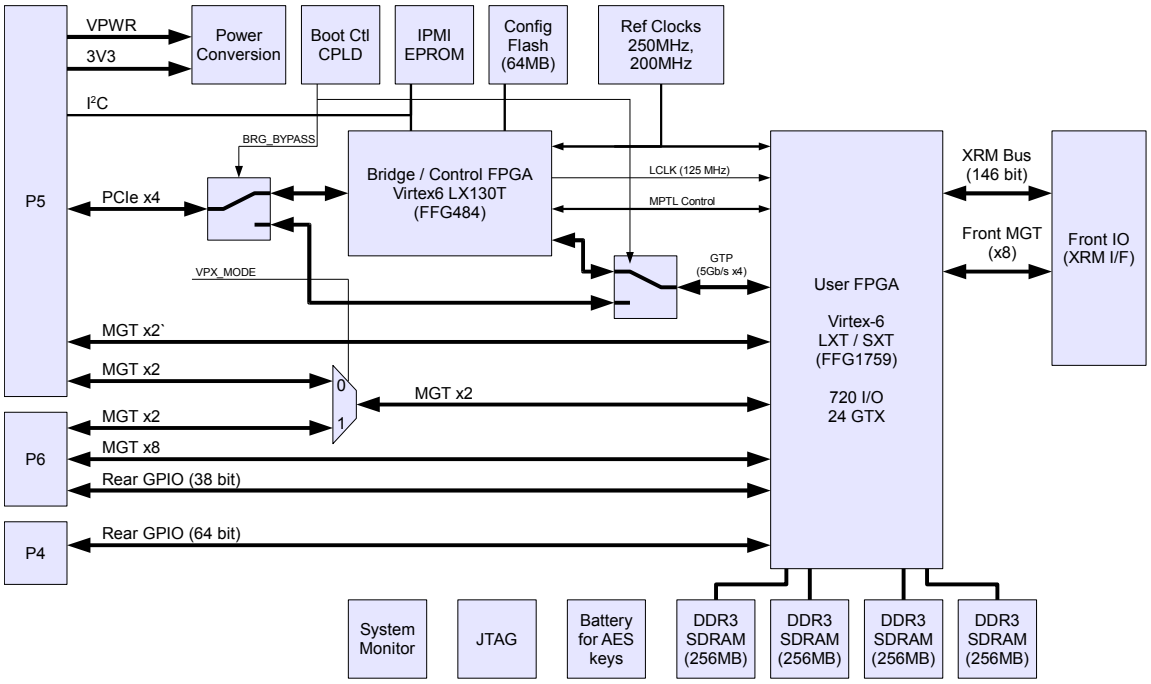


Figure 1: ADM-XRC-6T1 Block Diagram

3.1.1 Switch Definitions

There is a set of eight DIP switches placed on the rear of the board. Their functions are described in **Table 2 'Switch_Definitions'**.

> **Note:** All switches are OFF by default. All *Factory Test* and *Reserved* switches must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1-1	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the user FPGA.	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
SW1-2	*Factory Test*	Factory Test Mode	Normal Operation
SW1-3	E-Fuse	Enable E-Fuse programming voltage (VccEFuse = 2.5V)	Disable E-Fuse programming voltage (VccEFuse = 0V)
SW1-4	XMC JTAG	Connect JTAG chain to P5	Isolate JTAG chain from P5
SW1-5	One-time Configuration	Target FPGA is cleared then configured from Flash at power-up only.	Target FPGA is cleared then configured from flash at power-up and after every board reset (MRSTI#).

Table 2: Switch Definitions (continued on next page)

Switch Ref.	Function	ON State	Off State
SW1-6	Flash Boot Inhibit	Target FPGA is not configured from onboard flash memory.	Target FPGA is configured from on-board flash memory.
SW1-7	*Reserved*	-	-
SW1-8	VPX Mode	Connect Tgt RearMGT(7:6) to P6	Connect Tgt RearMGT(7:6) to P5

Table 2: Switch Definitions

3.1.2 LED Definitions

There are eight LEDs placed on the rear of the board to indicate the status:

Comp. Ref.	Function	ON State	Off State
D10 (Green)	Power Good	1.0V, 2.5V, 1.8V and 1.5V power supplies are on.	1.0V, 2.5V, 1.8V and 1.5V power supplies are not all on or all at their correct levels.
D11 (Green)	Bridge Done	Bridge FPGA is configured	Bridge FPGA is unconfigured
D12 (Green)	Target Done	Target FPGA is configured	Target FPGA is unconfigured
D9 (Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories.
D14 (Amber)	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the user FPGA	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
D8 (Amber)	XMC JTAG	On-board JTAG chain connected to P5	On-board JTAG chain is isolated from P5
D7 (Amber)	VPX Mode	Tgt RearMGT(7:6) are connected to P6	Tgt RearMGT(7:6) are connected to P5
D13 (Red)	Fault	Voltage or Temperature Fault Detected.	No fault detected

Table 3: LED Definitions

3.2 XMC Platform Interface

3.2.1 IPMI I2C

A 4 Kbit I2C EEPROM (type M24C04) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

3.2.2 MBIST#

Built-In Self Test. This output signal is driven active (low) until the FPGA with PCIe interface is configured. In normal operation, this is the bridge FPGA. In Bridge Bypass mode, it is the target FPGA.

3.2.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D7.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the target FPGA at pin AD30.

3.2.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier. When asserted, the bridge FPGA will be reset. At the end of the reset, the target FPGA configuration sequence will start. (See **Section 3.6 'Configuration'**.)

The MRSTI# signal is translated to 2.5V levels and connected to the target FPGA at pin AC30.

3.2.5 MRSTO#

XMC Reset Out. This optional output signal is unused and undriven.

3.2.6 MPRESENT#

Module Present. This output signal is connected directly to 0V.

3.3 JTAG Interface

3.3.1 On-board Interface

A JTAG boundary scan chain is connected to header J3. This allows the connection of the Xilinx™ JTAG cable for FPGA debug using the Xilinx ChipScope tools.

The JTAG Header pinout is shown in **Figure 2 'JTAG_Header_J2'**:

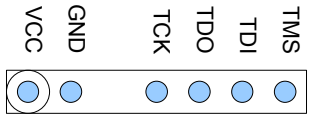


Figure 2: JTAG Header J2

The scan chain is shown in **Figure 3 'JTAG_Boundary_Scan_Chain'**:

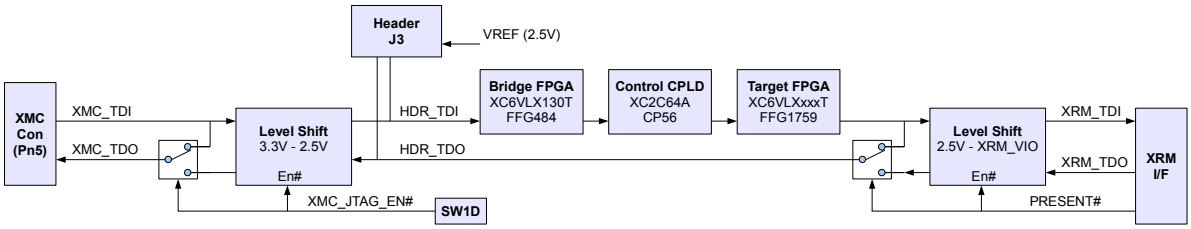


Figure 3: JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the XMC connector (SW1-4 is ON), Header J3 should not be used.

3.3.2 XMC Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The interface can be connected to the on-board interface (through level-translators) by switching SW1-4 ON. See **Section 3.1.1 'Switch_Definitions'**

3.3.3 JTAG Voltages

The on-board JTAG scan chain uses 2.5V. The Vcc supply provided on J3 to the JTAG cable is +2.5V and is protected by a poly fuse rated at 350mA. 3.3V signals must not be used at header J3.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the XRM interface use the adjustable voltage XRM_VIO.

3.4 Clocks

The **ADM-XRC-6T1** provides a wide variety of clocking options. The fixed reference clocks on the board can be combined with the PLLs in the FPGA to suit the target application.

The on-board clocks are detailed below.

Note: Clock Termination
The LVDS clocks do not have termination resistors on the circuit board. On-die terminations in the FPGA must be enabled by setting the attribute "DIFF_TERM = TRUE". This can either be set in the source code when instantiating the buffer, or in the User Constraints File (UCF). See the Xilinx™ Virtex-6 Libraries Guide and Constraints Guide for further details.

3.4.1 REFCLK200M

The fixed 200MHz reference clock REFCLK200M is a differential clock signal using LVDS. It is connected to a Global Clock input on the Target FPGA at pins AE30 and AF30.

This clock can be used to generate application-specific clock frequencies using the PLLs within the Virtex-6 FPGA. It is also suitable as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK200M	IO_L0_GC_24	LVDS_25	AE30	AF30

Table 4: REFCLK200M Connections

3.4.2 PCIe Reference Clock (PCIEREFCLK)

The 100MHz PCI Express® reference clock is provided by the carrier card through the Primary XMC connector, P5 at pins A19 and B19. This is multiplied to 250MHz and distributed to both the Bridge and Target FPGAs. On the Target FPGA, it is connected to GTX Quad 113 and 114 to allow its use as a reference for all the MGT links to the XMC connectors. (See **Figure 6 'MGT_Clocks'** for details of the MGT reference clocks.)

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK_1	MGTREFCLK1_113	LVDS_25	AD8	AD7
PCIEREFCLK_2	MGTREFCLK0_114	LVDS_25	AB8	AB7

Table 5: PCIEREFCLK Connections

3.4.3 REFCLK250M

The fixed 250.0MHz reference clock REFCLK250M, is a differential clock signal using LVDS. The clock is buffered and connected to three MGTREFCLK0 inputs on the Target FPGA at GTX Quad 113, 115 and 116. (See **Figure 6 'MGT_Clocks'**.)

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK250M_3	MGTREFCLK0_113	LVDS_25	AF8	AF7
REFCLK250M_2	MGTREFCLK0_115	LVDS_25	V8	V7
REFCLK250M_1	MGTREFCLK0_116	LVDS_25	M8	M7

Table 6: REFCLK250M Connections

3.4.4 GCLK_M2C

The clock "GCLK_M2C" is a differential clock signal using LVDS. It is provided by an XRM module through the XRM connector, CN1, at pins 110 & 108. It is connected to a Global Clock input on the Target FPGA.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
GCLK_M2C	IO_L1_GC_24	LVDS_25	W30	V30

Table 7: GCLK_M2C Connections

3.4.5 MGTCLK_M2C

The reference clock "MGTCLK_M2C" is a differential clock signal using LVDS. The clock is provided by an XRM module through the XRM connector, CN1, at pins 109 & 111. It is connected to GTX Quad 117 on the Target FPGA for application specific frequencies / line rates.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
MGTCLK_M2C	MGTREFCLK0_117	LVDS_25	G10	G9

Table 8: MGTCLK_M2C Connections

3.5 Flash Memory

A 512Mb Flash Memory (Intel / Numonyx PC28F512P30EF) is used to store board Vital Product Data (VPD), programmable clock parameters and configuration bitstreams for the Bridge and Target FPGAs.

The flash memory cannot be accessed by the target FPGA. Host access is only possible through the FLCTL, FLPAGE and FLDATA registers in the bridge FPGA.

Utilities for erasing, programming and verification of the flash memory are provided in the ADMXRC SDK.

Write Protect

The Flash Write Protect (WP#) pin is connected to an inverted version of the MVMRO signal at the XMC interface. When the MVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED, D9.

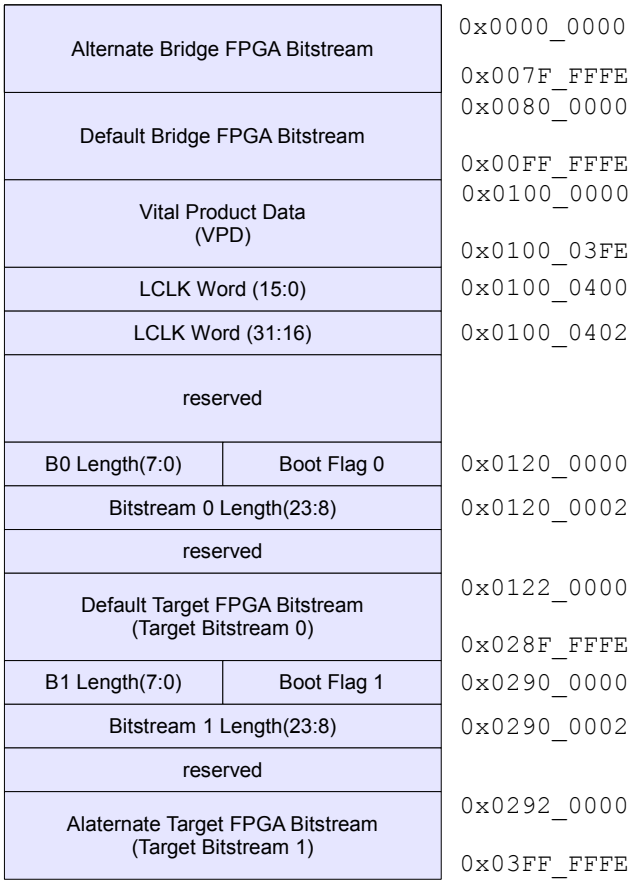


Figure 4: Flash Memory Map

3.6 Configuration

3.6.1 Power-Up Sequence

If valid data is stored in the flash memory, the bridge will automatically set the programmable clock generator and configure the Target FPGA at power-up.

This sequence can be inhibited by turning the Flash Boot Inhibit (FBI) switch, SW1-6 to ON. (See **Table 2 'Switch_Definitions'**).

Note: If an over-temperature alert is detected from the System Monitor, the target **will be cleared** by pulsing its PROG signal. See **Section 3.7.1 'Automatic_Temperature_Monitoring'**.

3.7 Health Monitoring

The **ADM-XRC-6T1** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using a National Semiconductor LM87, connected to control logic in the bridge FPGA using I2C.

The control logic scans the LM87 when instructed by host software and stores the measurements in a blockram. This allows the values to be read without the need to communicate directly with the LM87.

The following voltage rails and temperatures are monitored:

Monitor	*Purpose*
1.0V	FPGA Core Supply (VccINT)
1.5V	DDR3 SDRAM, Target FPGA memory I/O
1.8V	Flash Memory, DC-DC converters for GTX Supplies
2.5V	FPGA Auxiliary Supply (VccAUX)
XRM_VIO	XRM (Front-Panel) I/O voltage
3.3V	Board Input Supply
5.0V	Internally generated 5V supply
VPWR	Board Input Supply (either 5.0V or 12.0V)
Temp1	Target FPGA on-die temperature
Temp2	LM87 on-die temperature

Table 9: Voltage and Temperature Monitors

An example application that reads the system monitor ("sysmon") is available on request.

3.7.1 Automatic Temperature Monitoring

At power-up, the control logic sets temperature limits and enables the over-temperature interrupting the LM87. If the One-Time Configuration OTC function is disabled (using SW1-5, see **Table 2 'Switch_Definitions'**), the limits and interrupt will be re-set after a board reset (MRSTI#). If OTC is enabled, the limits and interrupt will only be set once at power-up.

The temperature limits are shown in **Table 10 'Temperature_Limits'**:

	Target FPGA		Board (LM87)	
	Min	Max	Min	Max
Commercial	0°C	+85°C	0°C	+70°C
Industrial	-40°C	+100°C	-40°C	+85°C

Table 10: Temperature Limits

Important:

If any temperature limit is exceeded, the Target FPGA is automatically cleared. This is indicated by Green LED D13 (Target DONE) switching off and Red LED, D14 (Fault) switching on.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

3.8 Local Bus

A Multiplexed Packet Transport Link (MPTL) connects the Bridge and Target FPGAs. It is capable of transferring data at up to 2GB/s simultaneously in each direction.

The MPTL replaces the parallel local bus used in previous generations of the ADM-XRC series. Details of the link and example designs are given in the Software Development Kit (SDK).

3.9 Target FPGA

3.9.1 I/O Bank Voltages

The Target FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in **Table 11 'Target_FPGA_IO_Banks'**. Full details of the IOSTANDARD required for each signal are given in the SDK.

IO Banks	Voltage	Purpose
0, 24	2.5V	Configuration, JTAG, LBus Control,XMC Control,Target SelectMap Interface
33,34	2.5V	Pn4
37, 36, 26, 25	1.5V	DRAM Banks 0 & 1
27	1.5V	DRAM Banks 0 XMC GPIO
13, 12	1.5V	DRAM Bank 2, XMC GPIO
23, 32, 22	1.5V	DRAM Banks 2 & 3
14, 15, 16, 17	XRM_VIO	XRM Interface (variable voltage)

Table 11: Target FPGA IO Banks (continued on next page)

IO Banks	Voltage	Purpose
21, 28, 38	1.5V	reserved

Table 11: Target FPGA IO Banks

3.9.2 Target MGT Links

There are a total of 24 Multi-Gigabit Transceiver (MGT) links connected to the Target FPGA:

Links	Width	Connection
RearMGT(3:0)	4	Bridge FPGA (for MPTL) or XMC Connector P5 lanes (3:0) in Bridge Bypass Mode
RearMGT(5:4)	2	Direct link to XMC P5 lanes (5:4)
RearMGT(7:6)	2	Link to XMC P5, lanes (7:6) in default mode, connector P6 lanes (9:8) in VPX mode.
RearMGT(15:8)	8	Direct link to XMC P6 lanes (7:0)
FrontMGT(7:0)	8	Direct link to XRM interface

Table 12: Target MGT Links

The connections of these links are shown in **Figure 5 'MGT_Links'**:

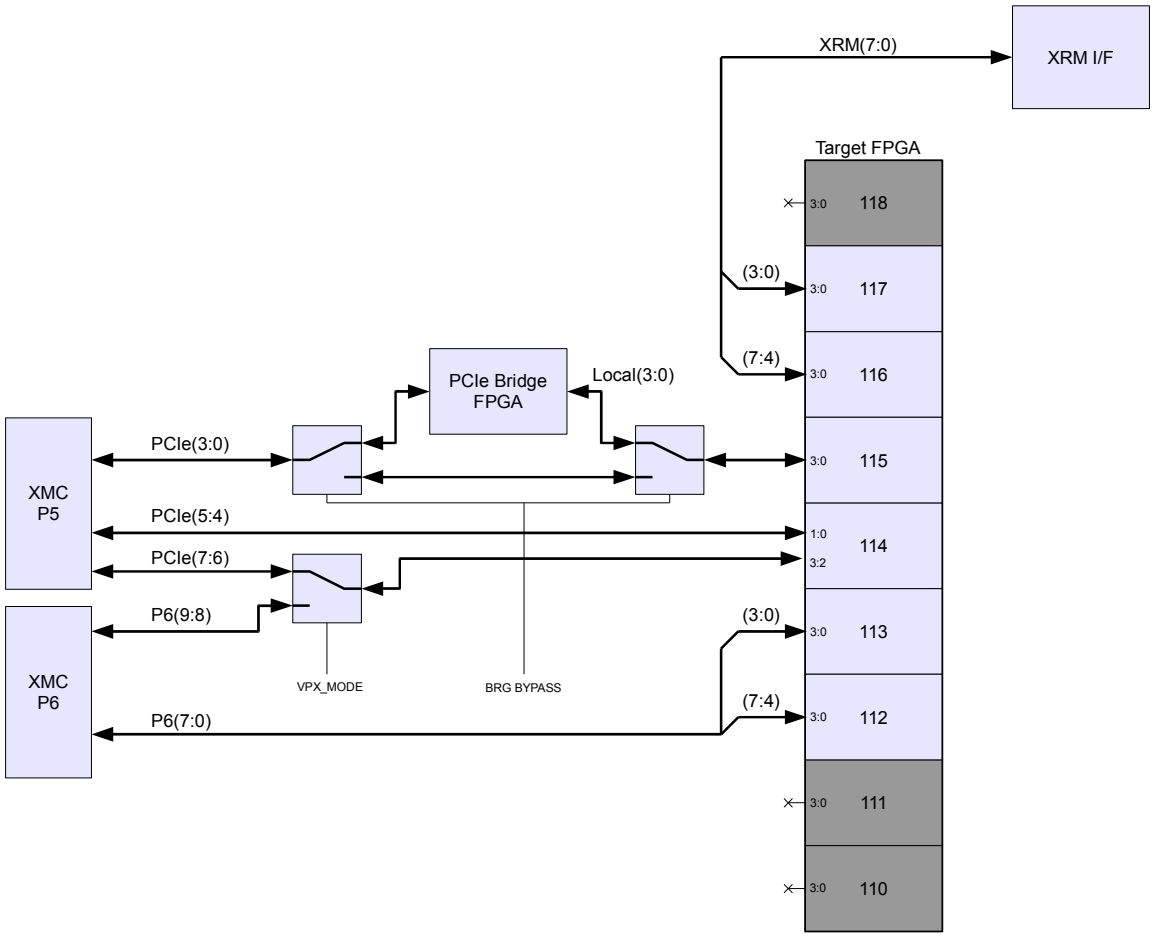


Figure 5: MGT Links

Notes:

(1) The numbering in the Target FPGA refers to the GTX Quad number. Each Quad contains a grouping of four **GTXE1** Multi-Gigabit Transceivers and two dedicated reference clock pairs.

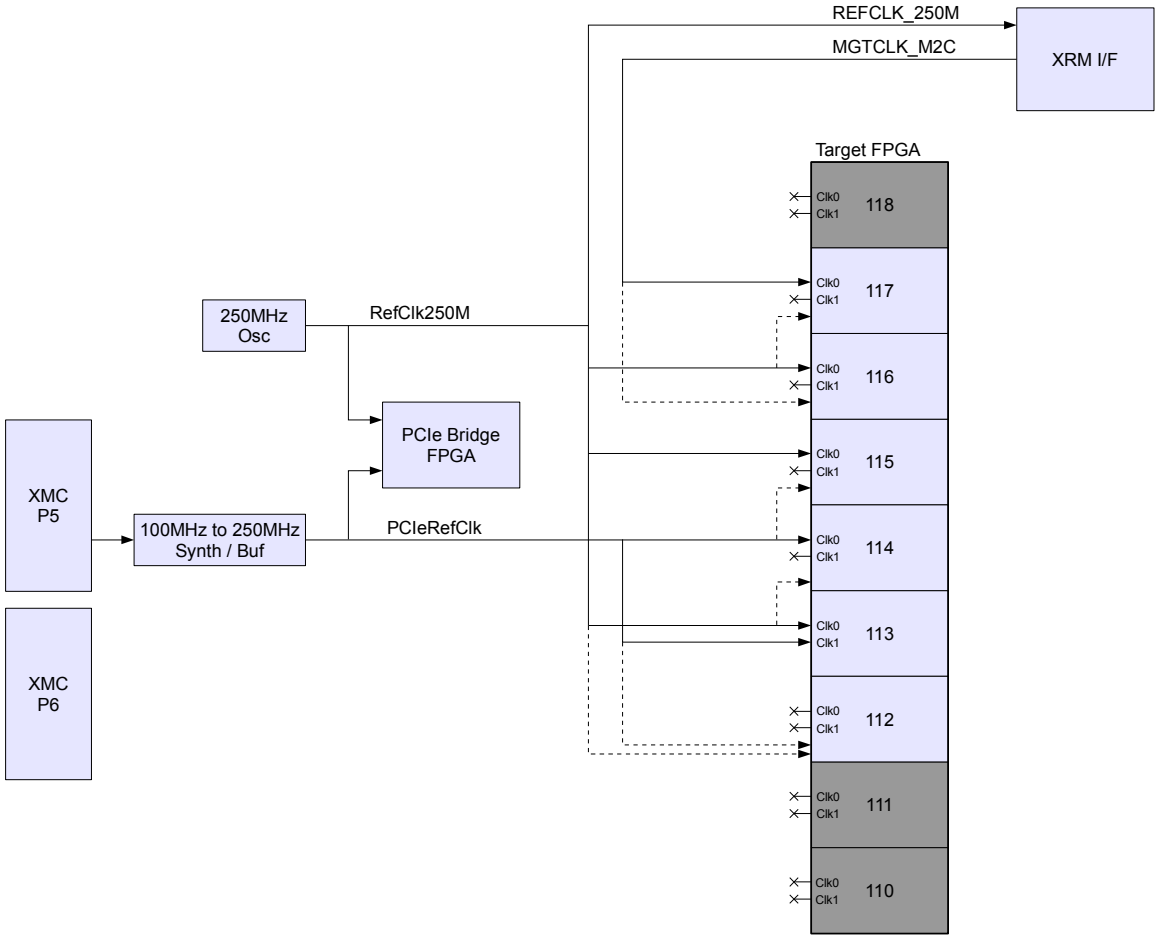


Figure 6: MGT Clocks

3.10 Memory Interfaces

The **ADM-XRC-6T1** has four independent banks of DDR3 SDRAM. Each bank consists of two 16 bit wide memory devices in parallel to provide a 32 bit datapath capable of running up to 400MHz (DDR-800). 1Gb devices (Micron MT41J64M16-187E) are fitted as standard to provide 256MB per bank. 2Gb devices (giving 512MB per bank) are available as an ordering option.

The memory banks are arranged for compatibility with the Xilinx™ Memory Interface Generator (MIG). **Figure 7 'DRAM_Banks'** Shows the component references and FPGA banks used. Full details of the interface, signaling standards and an example design are provided in the SDK.

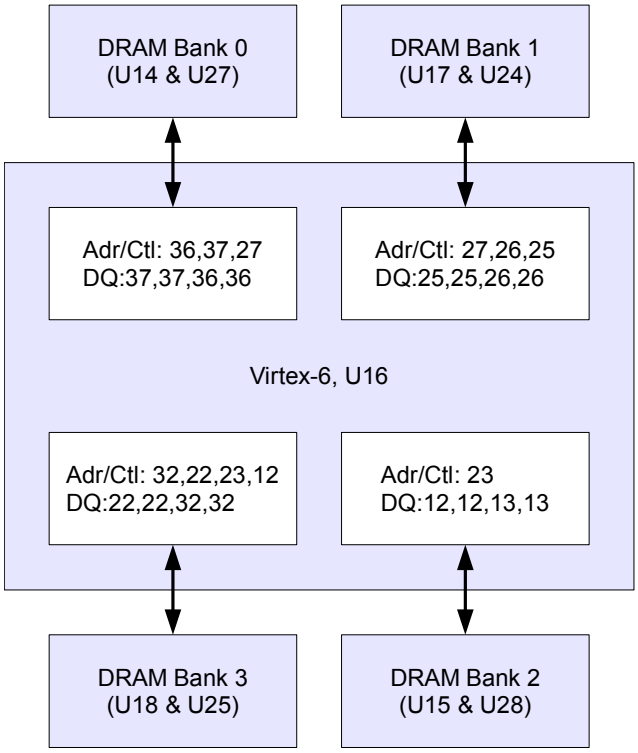


Figure 7: DRAM Banks

3.11 XRM Interface and Front-Panel I/O

The XRM interface provides a high-performance and flexible front-panel interface through a range of interchangeable XRM modules. Further details of the XRM modules can be found on the Alpha Data website.

The XRM interface consists of two samtec connectors, CN1 and CN2.

3.11.1 XRM Connector, CN1

Connector CN1 is for general-purpose signals, power and module control. The connector is a 180-way Samtec connector with 3 fields.

The part fitted to the **ADM-XRC-6T1** is Samtec QSH-090-01-F-D-A-K.

Full pinout information for this connector is listed in **Appendix B1 'XRM_Connector_CN1_Field_1'** to **Appendix B3 'XRM_Connector_CN1_Field_3'**.

3.11.2 XRM Connector CN2

Connector CN2 is for the high-speed serial (MGT) links.

The part fitted to the **ADM-XRC-6T1** is Samtec QSE-014-01-F-D-DP-A-K.

Full pinout information for this connector is listed in **Appendix B4 'XRM_Connector_CN2'**.

3.11.3 XRM I/F - GPIO

The general purpose IO (GPIO) signals are connected in 4 groups to the Target FPGA. Each group consists of 16 standard I/O pairs, a Regional Clock Capable pair and either 2 or 4 single-ended signals. There are no on-board terminations on the pairs and any can be used in single-ended modes.

To allow fast data transfer, all of the GPIO signals within a group are delay matched to within 100ps.

All the XRM GPIO signals and FPGA IO banks share a common voltage, XRM_VIO, that van be either 2.5V, 1.8V or 1.5V. The required voltage is stored within the platform management PROM on the XRM.

Group	FPGA Bank	Name	Function
Group A	17	XRM_DA (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DA_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SA (1:0)	2 single-ended GPIO
Group B	16	XRM_DB (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DB_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SB (1:0)	2 single-ended GPIO
Group C	15	XRM_DC (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DC_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SC (1:0)	2 single-ended GPIO
Group D	14	XRM_DD (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DD_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SD (3:0)	4 single-ended GPIO

Table 13: XRM GPIO Groups

3.11.4 XRM I/F - High-speed Serial Links

Eight MGT links are routed between the Target FPGA and the XRM interface. Lanes (6:0) are routed through the Samtec QSE-DP connector, CN2. Lane (7) is routed through the Samtec QSH connector, CN1.

Appendix A: Rear Connector Pinouts

A.1: Primary XMC Connector, P5

	A	B	C	D	E	F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR(6)
2	GND	GND	XMC_TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR(6)
4	GND	GND	XMC_TCK	GND	GND	MRSTO#
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR(6)
6	GND	GND	XMC_TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR(6)
8	GND	GND	XMC_TDI(4)	GND	GND	-12V
9	-	-	-	-	-	VPWR(5)
10	GND	GND	XMC_TDO(4)	GND	GND	GA0
11	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR(6)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	(5)	PER0p3	PER0n3	VPWR(6)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	-	PER0p5	PER0n5	VPWR(6)
16	GND	GND	MVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	-	PER0p7	PER0n7	-
18	GND	GND	-	GND	GND	-
19	REFCLK+0	REFCLK-0	-	WAKE#	ROOT0#	-
Notes:	(1) PCIe Channel 0 Lanes (3:0) are connected to the Bridge FPGA by default but can be routed to the target FPGA in Bridge Bypass Mode.					
	(2) PCIe Channel 0 Lanes (7:4) are only connected to the Target FPGA. This may be used as a second, 4-lane channel if supported by the carrier card, although this configuration is non-standard.					
	(3) PCIe Channel 0 Lanes (7:6) are not available when the board is in VPX Mode.					
	(4) JTAG is unused. XMC_TDI is connected to XMC_TDO.					
	(5) 3.3V AUX is unused.					
	(6) VPWR can be either +5V or +12V.					

Table A1: XMC Connector P5

A.2: Secondary XMC Connector, P6

	A	B	C	D	E	F
1	P6_TXp0	P6_TXn0	GPIO_37	P6_TXp1	P6_TXn1	GPIO_38
2	GND	GND	GPIO_35	GND	GND	GPIO_36
3	P6_TXp2	P6_TXn2	GPIO_33	P6_TXp3	P6_TXn3	GPIO_34
4	GND	GND	GPIO_31	GND	GND	GPIO_32
5	P6_TXp4	P6_TXn4	GPIO_29	P6_TXp5	P6_TXn5	GPIO_30
6	GND	GND	GPIO_27	GND	GND	GPIO_28
7	P6_TXp6	P6_TXn6	GPIO_25	P6_TXp7	P6_TXn7	GPIO_26
8	GND	GND	GPIO_23	GND	GND	GPIO_24
9	P6_TXp8	P6_TXn8	GPIO_21	P6_TXp9	P6_TXn9	GPIO_22
10	GND	GND	GPIO_19	GND	GND	GPIO_20
11	P6_RXp0	P6_RXn0	GPIO_17	P6_RXp1	P6_RXn1	GPIO_18
12	GND	GND	GPIO_15	GND	GND	GPIO_16
13	P6_RXp2	P6_RXn2	GPIO_13	P6_RXp3	P6_RXn3	GPIO_14
14	GND	GND	GPIO_11	GND	GND	GPIO_12
15	P6_RXp4	P6_RXn4	GPIO_9	P6_RXp5	P6_RXn5	GPIO_10
16	GND	GND	GPIO_7	GND	GND	GPIO_8
17	P6_RXp6	P6_RXn6	GPIO_5	P6_RXp7	P6_RXn7	GPIO_6
18	GND	GND	GPIO_3	GND	GND	GPIO_4
19	P6_RXp8	P6_RXn8	GPIO_1	P6_RXp9	P6_RXn9	GPIO_2
Notes:	(1) MGT Lanes P6_TX(7:0) and P6_RX(7:0) are connected directly to the Target FPGA.					
	(2) MGT Lanes P6_TX(9:8) and P6_RX(9:8) are only available in VPX Mode.					
	(3) GPIO signals are single-ended and 3.3V compatible.					

Table A2: XMC Connector P6

A.3: PMC Connector, P4

The PMC Connector, P4, is fitted as standard but can be omitted if required. 64 GPIO signals are connected between P4 and the target FPGA via FET bus switches. By limiting the signal voltage at 2.5V, these allow the use of 3.3V or 2.5V signalling levels to be used at P4.

Signals may be used in single-ended or as differential pairs.

Signal	FPGA	Pin P4	Pin P4	Pin FPGA Pin	Signal
PN4_P1	BA16	1	2	AV16	PN4_P2
PN4_N1	BA17	3	4	AW16	PN4_N2
PN4_P3	AY15	5	6	AR14	PN4_P4
PN4_N3	AW15	7	8	AT14	PN4_N4
PN4_P5	AN14	9	10	AM13	PN4_P6
PN4_N5	AN13	11	12	AM12	PN4_N6
PN4_P7	AP11	13	14	AP13	PN4_P8
PN4_N7	AP12	15	16	AR13	PN4_N8
PN4_P9	AR12	17	18	AU12	PN4_P10
PN4_N9	AT12	19	20	AU13	PN4_N10
PN4_P11	AV13	21	22	AW12	PN4_P12
PN4_N11	AV14	23	24	AW13	PN4_N12
PN4_P13	BB13	25	26	BB16	PN4_P14
PN4_N13	BB14	27	28	BB17	PN4_N14
PN4_P15	BA15	29	30	AV15	PN4_P16
PN4_N15	BA14	31	32	AU14	PN4_N16
PN4_P17	AJ16	33	34	AK18	PN4_P18
PN4_N17	AJ15	35	36	AJ18	PN4_N18
PN4_P19	AM17	37	38	AJ17	PN4_P20
PN4_N19	AM18	39	40	AK17	PN4_N20
PN4_P21	AL17	41	42	AK15	PN4_P22
PN4_N21	AL16	43	44	AK14	PN4_N22
PN4_P23	AN18	45	46	AN16	PN4_P24
PN4_N23	AN19	47	48	AM16	PN4_N24
PN4_P25	AP18	49	50	AP16	PN4_P26
PN4_N25	AR19	51	52	AP17	PN4_N26
PN4_P27	AT17	53	54	AU19	PN4_P28
PN4_N27	AU18	55	56	AT19	PN4_N28
PN4_P29	AV18	57	58	AY18	PN4_P30
PN4_N29	AV19	59	60	AW18	PN4_N30
PN4_P31	BA19	61	62	BB18	PN4_P32
PN4_N31	AY19	63	64	BB19	PN4_N32

Table A3: PMC Connector, P4

A.4: Rear MGT Connections to the Target FPGA

In normal mode, the target FPGA RearMGT lanes (3:0) are connected to the Bridge FPGA. In Bridge Bypass Mode, they are connected to P5 lanes (3:0).

RearMGT Lanes (5:4) are connected directly to P5 lanes (5:4)

In normal mode, Lanes (7:6) are connector to P5 lanes (7:6). In VPX Mode, they are connected to P6 lanes (9:8). The pin mappings are as follows in **Table A4 'Target_RearMGT_Mapping'**

Signal	Tgt FPGA \"P\" Pin	Tgt FPGA \"N\" Pin
RearMGT_TX<0>	U1	U2
RearMGT_TX<1>	T3	T4
RearMGT_TX<2>	R1	R2
RearMGT_TX<3>	P3	P4
RearMGT_TX<4>	W1	W2
RearMGT_TX<5>	AA1	AA2
RearMGT_TX<6>	AC1	AC2
RearMGT_TX<7>	AE1	AE2
RearMGT_TX<8>	AG1	AG2
RearMGT_TX<9>	AH3	AH4
RearMGT_TX<10>	AJ1	AJ2
RearMGT_TX<11>	AK3	AK4
RearMGT_TX<12>	AL1	AL2
RearMGT_TX<13>	AM3	AM4
RearMGT_TX<14>	AN1	AN2
RearMGT_TX<15>	AP3	AP4
RearMGT_RX<0>	W5	W6
RearMGT_RX<1>	V3	V4
RearMGT_RX<2>	U5	U6
RearMGT_RX<3>	R5	R6
RearMGT_RX<4>	Y3	Y4
RearMGT_RX<5>	AA5	AA6
RearMGT_RX<6>	AB3	AB4
RearMGT_RX<7>	AC5	AC6
RearMGT_RX<8>	AD3	AD4
RearMGT_RX<9>	AE5	AE6
RearMGT_RX<10>	AF3	AF4
RearMGT_RX<11>	AG5	AG6
RearMGT_RX<12>	AJ5	AJ6
RearMGT_RX<13>	AL5	AL6
RearMGT_RX<14>	AM7	AM8

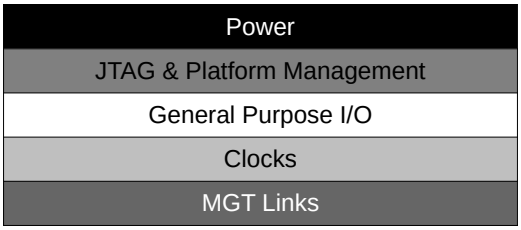
Table A4: Target RearMGT Mapping (continued on next page)

Signal	Tgt FPGA \"P\" Pin	Tgt FPGA \"N\" Pin
RearMGT_RX<15>	AN5	AN6

Table A4: Target RearMGT Mapping

Appendix B: Front (XRM) Connector Pinouts

The XRM interface consists of two connectors: CN1 and CN2. CN1 is a 180-way Samtec QSH in 3 fields. It is for general-purpose signals, power and module control. CN2 is a 28-way Samtec QSE-DP for high-speed serial (MGT) links.



B.1: XRM Connector CN1, Field 1

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DA_N0	N39	1	2	M39	DA_N1
DA_P0	N38	3	4	M38	DA_P1
DA_N2	T36	5	6	P40	DA_P3
DA_P2	U36	7	8	P41	DA_N3
DA_N4	L40	9	10	L42	DA_N5
DA_P4	L39	11	12	L41	DA_P5
DA_N6	T35	13	14	R42	DA_N7
DA_P6	T34	15	16	P42	DA_P7
DA_P8	R39	17	18	M41	DA_P9
DA_N8	P38	19	20	M42	DA_N9
DA_N10	P37	21	22	T40	DA_N11
DA_P10	N36	23	24	R40	DA_P11
DA_N12	R38	25	26	N40	DA_P13
DA_P12	T39	27	28	N41	DA_N13
DA_N14	M37	29	30	T41	DA_P15
DA_P14	M36	31	32	T42	DA_N15
DB_N0	Y37	33	34	V36	DB_N1
DB_P0	W37	35	36	W36	DB_P1
SA_0	N35	37	38	P36	DA_CC_P16
3V3	-	39	40	P35	DA_CC_N16
3V3	-	41	42	-	FORCE2V5_L
3V3	-	43	44	-	2V5
5V0	-	45	46	-	VREF
5V0	-	47	48	-	VccIO
VBATT	-	49	50	-	VccIO
12V0	-	51	52	-	VccIO
12V0	-	53	54	-	M12V0
PRESENCE_L	-	55	56	-	TDI
TCK	-	57	58	-	TRST
TMS	-	59	60	-	TDO

Table B1: XRM Connector CN1, Field 1

B.2: XRM Connector CN1, Field 2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DB_N2	V39	61	62	U34	DB_N3
DB_P2	U39	63	64	V34	DB_P3
DB_N4	U38	65	66	V35	DB_N5
DB_P4	U37	67	68	W35	DB_P5
DB_N6	U33	69	70	W38	DB_N7
DB_P6	U32	71	72	V38	DB_P7
DB_N8	U41	73	74	V40	DB_P9
DB_P8	U42	75	76	W40	DB_N9
DB_P10	V33	77	78	W41	DB_N11
DB_N10	W33	79	80	V41	DB_P11
DB_N12	Y39	81	82	W42	DB_P13
DB_P12	Y40	83	84	Y42	DB_N13
DB_N14	Y35	85	86	AA39	DB_N15
DB_P14	AA35	87	88	Y38	DB_P15
DB_CC_P16	W32	89	90	AA34	SB_1
DB_CC_N16	Y33	91	92	AC38	SC_0
SA_1	R35	93	94	AD36	SC_1
SB_0	AA36	95	96	AG38	SD_0
DC_CC_P16	AD32	97	98	AB38	DC_N1
DC_CC_N16	AE32	99	100	AB37	DC_P1
DC_N0	AB36	101	102	AH34	DD_CC_P16
DC_P0	AC36	103	104	AJ35	DD_CC_N16
SD_1A	G36	105	106	AH35	SD_3
SD_2A	J36	107	108	AF30	GCLK_M2C_N
MGTCLK_M2C_P	G10	109	110	AE30	GCLK_M2C_P
MGTCLK_M2C_N	G9	111	112	-	SDA
MGTCLK_C2M_N	-	113	114	-	SCL
MGTCLK_C2M_P	-	115	116	-	ALERT_N
MGT_C2M_P7	K3	117	118	J5	MGT_M2C_P7
MGT_C2M_N7	K4	119	120	J6	MGT_M2C_N7

Table B2: XRM Connector CN1, Field 2

B.3: XRM Connector CN1, Field 3

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DC_P2	AC41	121	122	AA42	DC_P3
DC_N2	AD41	123	124	AB42	DC_N3
DC_N4	AC33	125	126	AB39	DC_P5
DC_P4	AC34	127	128	AA40	DC_N5
DC_P6	AD42	129	130	AC40	DC_P7
DC_N6	AE42	131	132	AD40	DC_N7
DC_N8	AD33	133	134	AB41	DC_N9
DC_P8	AE33	135	136	AA41	DC_P9
DC_P10	AF42	137	138	AD38	DC_N11
DC_N10	AF41	139	140	AE38	DC_P11
DC_P12	AB32	141	142	AD37	DC_N13
DC_N12	AB33	143	144	AE37	DC_P13
DC_N14	AE39	145	146	AL42	DD_P1
DC_P14	AE40	147	148	AM42	DD_N1
DD_P0	AK38	149	150	AE35	DC_N15
DD_N0	AJ38	151	152	AE34	DC_P15
DD_P2	AJ42	153	154	AM41	DD_N3
DD_N2	AK42	155	156	AL41	DD_P3
DD_N4	AG37	157	158	AG41	DD_N5
DD_P4	AF37	159	160	AF40	DD_P5
DD_P6	AK40	161	162	AL39	DD_N7
DD_N6	AL40	163	164	AK39	DD_P7
DD_N8	AF36	165	166	AH41	DD_N9
DD_P8	AF35	167	168	AG42	DD_P9
DD_N10	AJ40	169	170	AJ41	DD_N11
DD_P10	AH39	171	172	AH40	DD_P11
DD_N12	AF34	173	174	AG39	DD_N13
DD_P12	AG34	175	176	AF39	DD_P13
DD_N14	AG33	177	178	AK37	DD_N15
DD_P14	AF32	179	180	AJ37	DD_P15

Table B3: XRM Connector CN1, Field 3

B.4: XRM Connector CN2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
MGT_C2M_P0	J1	1	2	H7	MGT_M2C_P0
MGT_C2M_N0	J2	3	4	H8	MGT_M2C_N0
MGT_C2M_P1	H3	5	6	G5	MGT_M2C_P1
MGT_C2M_N1	H4	7	8	G6	MGT_M2C_N1
MGT_C2M_P4	N1	9	10	P7	MGT_M2C_P4
MGT_C2M_N4	N2	11	12	P8	MGT_M2C_N4
MGT_C2M_P5	M3	13	14	N5	MGT_M2C_P5
MGT_C2M_N5	M4	15	16	N6	MGT_M2C_N5
MGT_C2M_P2	G1	17	18	F7	MGT_M2C_P2
MGT_C2M_N2	G2	19	20	F8	MGT_M2C_N2
MGT_C2M_P3	F3	21	22	E5	MGT_M2C_P3
MGT_C2M_N3	F4	23	24	E6	MGT_M2C_N3
MGT_C2M_P6	L1	25	26	L5	MGT_M2C_P6
MGT_C2M_N6	L2	27	28	L6	MGT_M2C_N6

Table B4: XRM Connector CN2

Appendix C: XRM-IO146 Pinout

The following tables detail the pin-out of the Mictor connector on the XRM-IO146 when fitted to an **ADM-XRC-6TL**.

Signal	FPGA	Samtec	Mictor	Mictor	Samtec	FPGA	Signal
DA_P0	N38	3	1	2	6	P40	DA_P3
DA_N0	N39	1	3	4	8	P41	DA_N3
DA_P2	U36	7	5	6	4	M38	DA_P1
DA_N2	T36	5	7	8	2	M39	DA_N1
DA_P4	L39	11	9	10	12	L41	DA_P5
DA_N4	L40	9	11	12	10	L42	DA_N5
DA_P6	T34	15	13	14	16	P42	DA_P7
DA_N6	T35	13	15	16	14	R42	DA_N7
DA_P8	R39	17	17	18	18	M41	DA_P9
DA_N8	P38	19	19	20	20	M42	DA_N9
DA_P10	N36	23	21	22	24	R40	DA_P11
DA_N10	P37	21	23	24	22	T40	DA_N11
DA_P12	T39	27	25	26	26	N40	DA_P13
DA_N12	R38	25	27	28	28	N41	DA_N13
DA_P14	M36	31	29	30	30	T41	DA_P15
DA_N14	M37	29	31	32	32	T42	DA_N15
SA_0	N35	37	33	34	38	P36	DA_CC_P16
SA_1	R35	93	35	36	40	P35	DA_CC_N16
+5V	-	-	37	38	90	AA34	SB_1

Table C1: XRM-IO146 Pinout, pins 1 - 38

Signal	FPGA	Samtec	Mictor	Mictor	Samtec	FPGA	Signal
DB_P0	W37	35	39	40	36	W36	DB_P1
DB_N0	Y37	33	41	42	34	V36	DB_N1
DB_P2	U39	63	43	44	64	V34	DB_P3
DB_N2	V39	61	45	46	62	U34	DB_N3
DB_P4	U37	67	47	48	68	W35	DB_P5
DB_N4	U38	65	49	50	66	V35	DB_N5
DB_P6	U32	71	51	52	72	V38	DB_P7
DB_N6	U33	69	53	54	70	W38	DB_N7
DB_P8	U42	75	55	56	74	V40	DB_P9
DB_N8	U41	73	57	58	76	W40	DB_N9
DB_P10	V33	77	59	60	80	V41	DB_P11
DB_N10	W33	79	61	62	78	W41	DB_N11
DB_P12	Y40	83	63	64	82	W42	DB_P13
DB_N12	Y39	81	65	66	84	Y42	DB_N13
DB_P14	AA35	87	67	68	88	Y38	DB_P15
DB_N14	Y35	85	69	70	86	AA39	DB_N15
SD_1	AG36	105	71	72	89	W32	DB_CC_P16
SD_2	AJ36	107	73	74	91	Y33	DB_CC_N16
+5V	-	-	75	76	95	AA36	SB_0

Table C2: XRM-IO146 Pinout, pins 39 - 76

Signal	FPGA	Samtec	Mictor	Mictor	Samtec	FPGA	Signal
DC_P0	AC36	103	77	78	100	AB37	DC_P1
DC_N0	AB36	101	79	80	98	AB38	DC_N1
DC_P2	AC41	121	81	82	122	AA42	DC_P3
DC_N2	AD41	123	83	84	124	AB42	DC_N3
DC_P4	AC34	127	85	86	126	AB39	DC_P5
DC_N4	AC33	125	87	88	128	AA40	DC_N5
DC_P6	AD42	129	89	90	130	AC40	DC_P7
DC_N6	AE42	131	91	92	132	AD40	DC_N7
DC_P8	AE33	135	93	94	136	AA41	DC_P9
DC_N8	AD33	133	95	96	134	AB41	DC_N9
DC_P10	AF42	137	97	98	140	AE38	DC_P11
DC_N10	AF41	139	99	100	138	AD38	DC_N11
DC_P12	AB32	141	101	102	144	AE37	DC_P13
DC_N12	AB33	143	103	104	142	AD37	DC_N13
DC_P14	AE40	147	105	106	152	AE34	DC_P15
DC_N14	AE39	145	107	108	150	AE35	DC_N15
SC_0	AC38	92	109	110	97	AD32	DC_CC_P16
SC_1	AD36	94	111	112	99	AE32	DC_CC_N16
+5V	-	-	113	114	-	-	+5V

Table C3: XRM-IO146 Pinout, pins 77 - 114

Signal	FPGA	Samtec	Mictor	Mictor	Samtec	FPGA	Signal
DD_P0	AK38	149	115	116	146	AL42	DD_P1
DD_N0	AJ38	151	117	118	148	AM42	DD_N1
DD_P2	AJ42	153	119	120	156	AL41	DD_P3
DD_N2	AK42	155	121	122	154	AM41	DD_N3
DD_P4	AF37	159	123	124	160	AF40	DD_P5
DD_N4	AG37	157	125	126	158	AG41	DD_N5
DD_P6	AK40	161	127	128	164	AK39	DD_P7
DD_N6	AL40	163	129	130	162	AL39	DD_N7
DD_P8	AF35	167	131	132	168	AG42	DD_P9
DD_N8	AF36	165	133	134	166	AH41	DD_N9
DD_P10	AH39	171	135	136	172	AH40	DD_P11
DD_N10	AJ40	169	137	138	170	AJ41	DD_N11
DD_P12	AG34	175	139	140	176	AF39	DD_P13
DD_N12	AF34	173	141	142	174	AG39	DD_N13
DD_P14	AF32	179	143	144	180	AJ37	DD_P15
DD_N14	AG33	177	145	146	178	AK37	DD_N15
SD_0	AG38	96	147	148	102	AH34	DD_CC_P16
SD_3	AH35	106	149	150	104	AJ35	DD_CC_N16
+5V	-	-	151	152	-	-	+5V

Table C4: XRM-IO146 Pinout, pins 115 - 152

INDEX

Revision History:

Date	Revision	Nature of Change
31/05/10	0.1	First Draft
16/06/10	1.0	First Issue

Address: 4 West Silvermills Lane,
Edinburgh, EH3 5BD, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 2570 North First Street, Suite 440
San Jose, CA 95131
Telephone: (408) 467 5076 General
(408) 916 5713 Sales
Fax: (408) 436 5524
(866) 820 9956 toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com